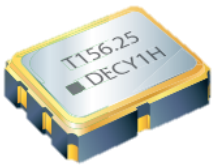
Product Features

1. Output Frequency：
   15~2100 MHz (LVPECL / LVDS)
   15~700 MHz (HCSL)
2. Frequency Stability ：
   ± 30 ppm @ (-40 ~ 85℃)
   ± 50 ppm @ (-40 ~ 105℃)
3. Supply Voltage ： 1.8 , 2.5 , 3.3V (Typ.)
4. Output Type ： LVPECL / LVDS / HCSL
5. Phase Jitter：
   0.15fs (Typ.) @156.25MHz LVPECL, 25℃
6. High Power Supply Noise Rejection Performance
7. Industry Standard Package：
   2.5 x 2.0 x 1.2 mm

Application：
- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch



Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications**

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
LVPECL / LVDS / HCSL Common Electrical Characteristics						
Nominal Frequency	F		15~2100		MHz	LVPECL / LVDS
			15~700			HCSL
Frequency Stability	ST		± 30		ppm	@ -40~85℃ , Note 1
			± 50			@ -40~105℃ , Note 1
Operating Temperature	Topr	-40	-	85	℃	
		-40	-	105		
Supply Voltage	Vdd		1.8 , 2.5 , 3.3 (± 10%)		V	Note 2
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
LVPECL Electrical Characteristics						
Current Consumption	Icc	-	93	106	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	91	104	uA	OE = Low
Output Voltage High	VoH	Vdd-1.165	-	Vdd-0.8	V	
Output Voltage Low	VoL	Vdd-2.0	-	Vdd-1.555	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7xVdd	-	-	V	Note 3 , (Logic 1)
Enable Voltage Low	-	-	-	0.3xVdd	V	Note 3 , (Logic 0)
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15~0.2	0.25	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note4

Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

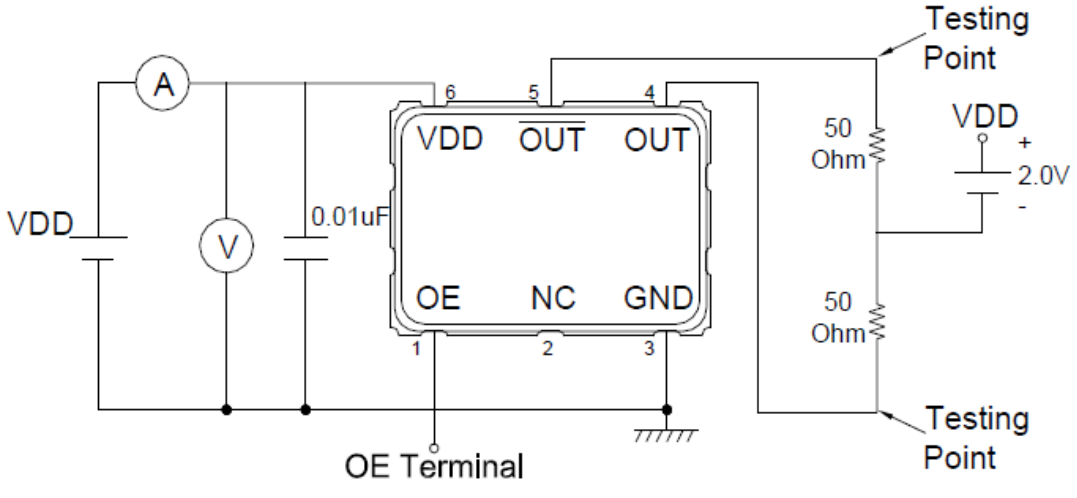
● Table 1 . Electrical Specifications (Continued)

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
LVDS Electrical Characteristics						
Current Consumption	Icc	-	69	80	mA	RL=100Ω
Standby Current	Icc(ST)	-	67	78	uA	OE = Low
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	Vdiff	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7xVdd	-	-	V	Note 3
Enable Voltage Low	-	-	-	0.3xVdd	V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15	0.25	ps	Integrated from 12KHz ~ 20MHz @150MHz , 3.3V , Note 4
HCSL Electrical Characteristics						
Current Consumption	Icc	-	-	30	mA	RL=33Ω and 49.9 Ω to GND
Standby Current	Icc(ST)	-	-	10	uA	OE = Low
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7xVdd	-	-	V	Note 3
Enable Voltage Low	-	-	-	0.3xVdd	V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.2	0.25	ps	Integrated from 12KHz ~ 20MHz @100MHz , 3.3V , Note 4

Note 1 : Inclusive of frequency tolerance at 25℃ , variation over temperature , supply voltage variation , 10 years aging and vibration.
Note 2 : LVPECL can not support VDD 1.8V .
Note 3 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.
Note 4 : Phase Jitter will be slightly different according to output frequency and supply voltage.

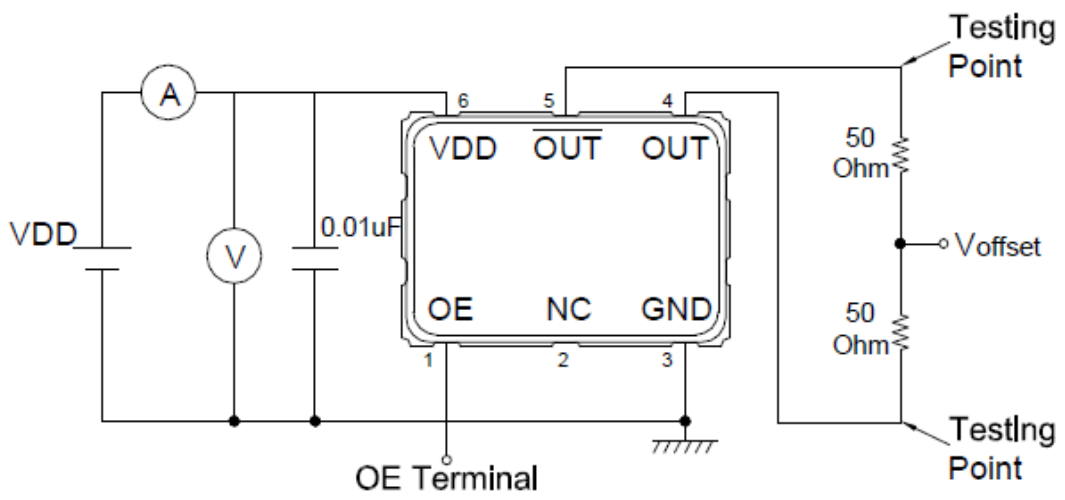
● Test Diagram

■ LVPECL

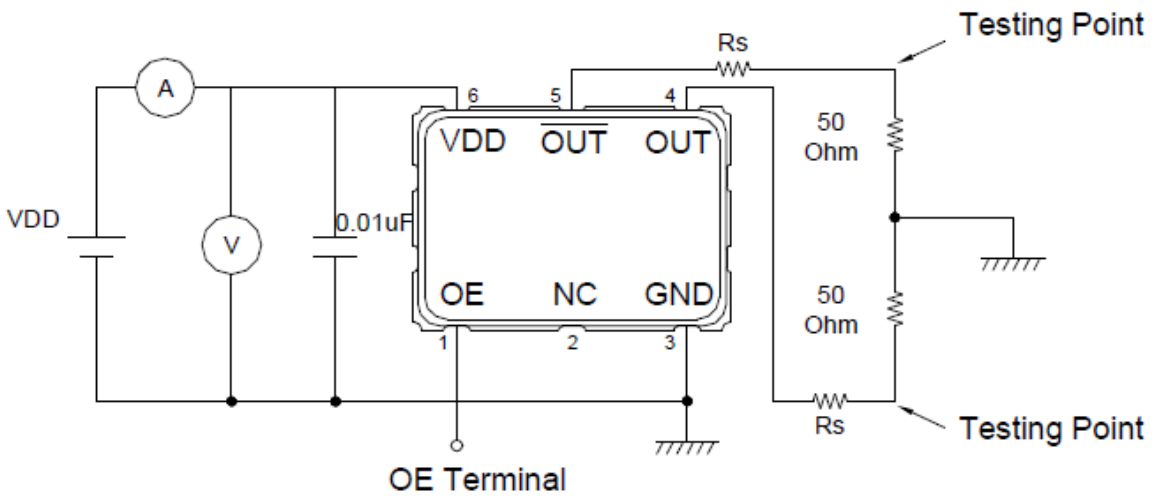


- **Test Diagram (Continued)**

■ **LVDS**



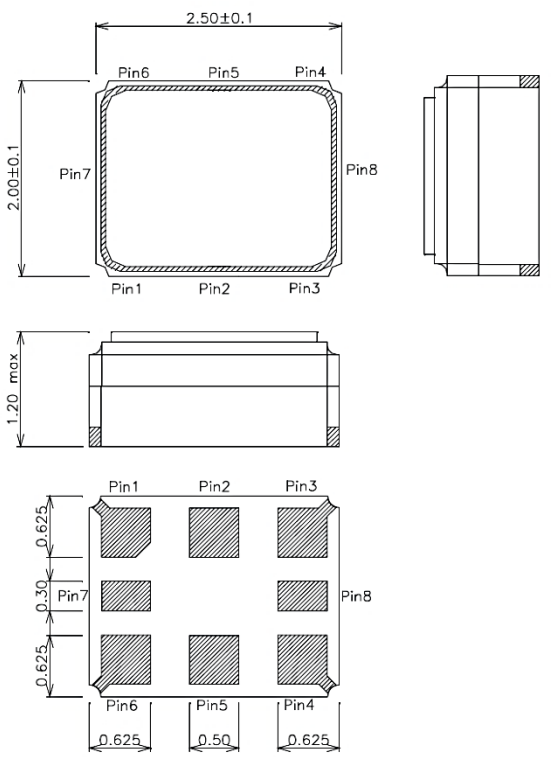
■ **HCSL**



Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All of the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.
4. HCSL RS= 0 Ohm for test. 0 Ohm to 33 Ohm to minimize overshoot and ringback effect in application.

- **Dimensions & Footprint (Recommended)**

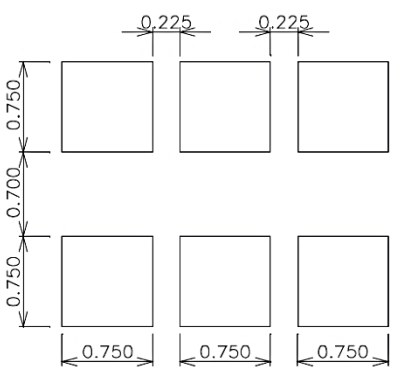


※ Pad dimension tolerance ±0.2 mm

Pin Function:

1. OE
2. NC
3. GND
4. OUT
5. $\overline{\text{OUT}}$
6. VDD
7. NC
8. NC

Land Pattern:



※ Power Supply Decoupling Capacitor is Required.